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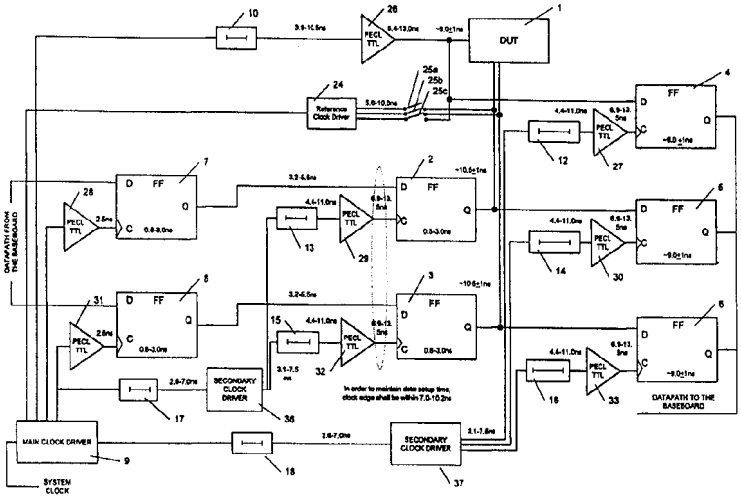

(57) Abstract

Automatic test equipment for memory device testing with means for providing a high accuracy of transferring and receiving signals when testing a semiconductor device under test (DUT) by intelligent skew calibration of a timing system. The means for automatic skew calibration of a transceiver comprises a plurality of input registers (2, 3) for transmitting signals; a plurality of output registers (4, 5, 6) for receiving signals; a main clock driver (9) for generating a main clock signal; a reference clock driver (24) for generating reference signals for calibrating the registers; the said reference clock driver (24) being associated with the said main clock driver (9); and a plurality of phase shift means (12, 13, 14, 15, 16) comprising at least one set of phase shift means associated with each said plurality of registers, for the relative alignment of the register's timing within each plurality. The calibration is performed using a common time base which is distributed by means of a transmission line having predetermined wave characteristics.